5812 ?

SN751508, SN751518
DC PLASMA DISPLAY DRIVERS

ADVANCE
INFORMATION

3 Display Drivers

TYPICAL CHARACTERISTICS

TRANSITION TIME, Q OUTPUT,
LOW TO HIGH
vs
FREE-AIR TEMPERATURE

$V_{CC} = 5$ V
$C_L = 15$ pF
$R_L = 91$ kΩ

t_{TLH} — Transition Time, Q Output, Low to High — μs

T_A — Free-Air Temperature — °C

FIGURE 7

TRANSITION TIME, Q OUTPUT,
HIGH TO LOW
vs
FREE-AIR TEMPERATURE

$V_{CC} = 5$ V
$C_L = 15$ pF
$R_L = 91$ kΩ

t_{THL} — Transition Time, Q Output, High to Low — μs

T_A — Free-Air Temperature — °C

FIGURE 8

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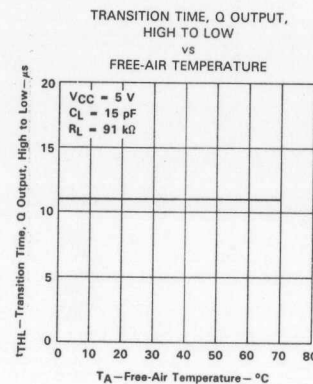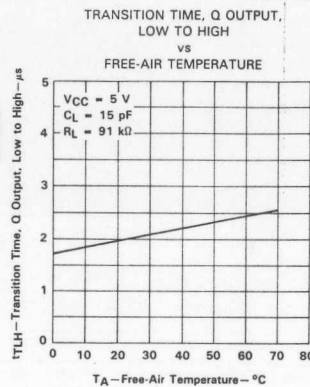
TL4810BI, TL4810B
VACUUM FLUORESCENT DISPLAY DRIVERS

D2715, DECEMBER 1984 — REVISED FEBRUARY 1985

- Each Device Drives 10 Lines
- 60-V Output Voltage Rating
- 40-mA Output Source Current
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Latches on All Driver Outputs
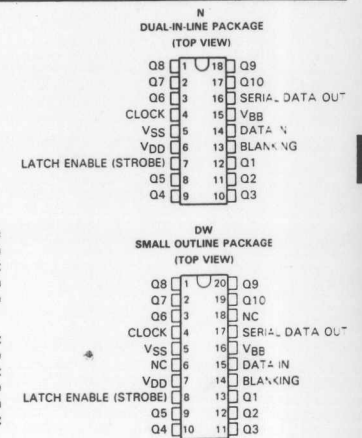- Improved Direct Replacement for UCN4810A and TL4810A

description

The TL4810BI and TL4810B are monolithic BIDFET[†] integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large display arrays.

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high and is latched when the latch enable is low. When the blanking input is high, all outputs are low.

Outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 volts and 40 milliamperes source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pull-up resistor to V_{DD} when driven by TTL logic.

The TL4810BI is characterized for operation from −40°C to 85°C. The TL4810B is characterized for operation from 0°C to 70°C.

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

```
         ___  ___
Q8    [ 1 U 18 ] Q9
Q7    [ 2    17 ] Q10
Q6    [ 3    16 ] SERIAL DATA OUT
CLOCK [ 4    15 ] VBB
VSS   [ 5    14 ] DATA IN
VDD   [ 6    13 ] BLANKING
LATCH ENABLE (STROBE) [ 7  12 ] Q1
Q5    [ 8    11 ] Q2
Q4    [ 9    10 ] Q3
```

DW
SMALL OUTLINE PACKAGE
(TOP VIEW)

```
         ___  ___
Q8    [ 1 U 20 ] Q9
Q7    [ 2    19 ] Q10
Q6    [ 3    18 ] NC
CLOCK [ 4    17 ] SERIAL DATA OUT
VSS   [ 5    16 ] VBB
NC    [ 6    15 ] DATA IN
VDD   [ 7    14 ] BLANKING
LATCH ENABLE (STROBE) [ 8  13 ] Q1
Q5    [ 9    12 ] Q2
Q4    [ 10   11 ] Q3
```
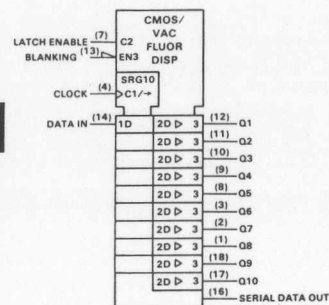
NC — No internal connection

3 Display Drivers

† BIDFET — Bipolar, Double-Diffused, N-Channel and P-Channel MOS transistors on same chip — patented process.

PRODUCTION DATA documents contain information
current as of publication date. Products conform to
specifications per the terms of Texas Instruments
standard warranty. Production processing does not
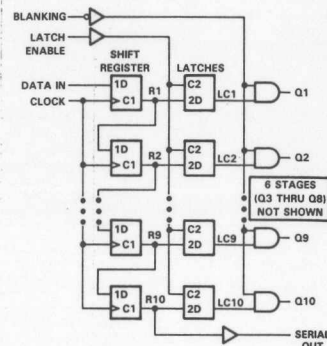necessarily include testing of all parameters.

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Display Drivers

3

logic symbol[†]

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and
IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)

typical operating sequence

schematics of inputs and outputs

FUNCTION TABLE

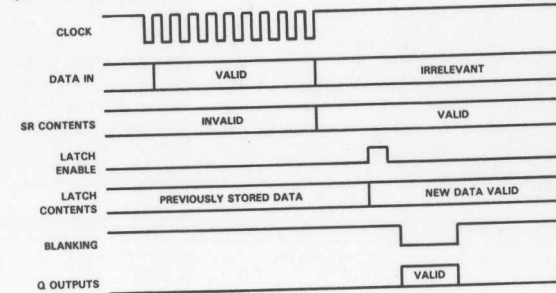| FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R10[‡]	LATCHES LC1 THRU LC10	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANK-ING			SERIAL	Q1 THRU Q10
LOAD	↑	X	X	Load and shift[‡]	Determined by Latch Enable[§]	R10	Determined by Blanking
	No↑	X	X	No change	Determined by Latch Enable[§]	R10	Determined by Blanking
LATCH	X	L	X	As determined above	Stored data	R10	Determined by Blanking
	X	H	X	As determined above	New data	R10	Determined by Blanking
BLANK	X	X	H	As determined above	Determined by Latch Enable[§]	R10	All L
	X	X	L	As determined above	Determined by Latch Enable[§]	R10	LC1 thru LC10 respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
‡ Register R10 takes on the state of R9, R9 takes on the state of R8 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
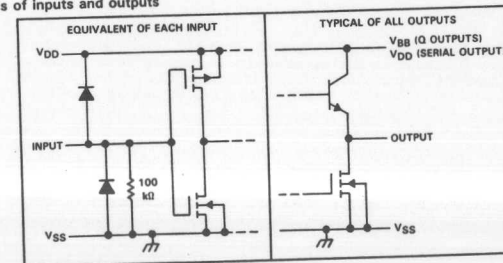§ New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{DD} (see Note 1)	18 V
Driver supply voltage, V_{BB}	70 V
Output voltage	70 V
Input voltage	-0.3 V to $V_{DD} + 0.3$ V
Continuous total dissipation at 25°C free air-temperature (see Note 2):	
DW package	1150 mW
N package	875 mW
Operating free-air temperature range: TL4810BI	-40°C to 85°C
TL4810B	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
DW	1150	9.2 mW/°C	25°C
N	875	7.0 mW/°C	25°C

recommended operating conditions

PARAMETER		TL4810BI			TL4810B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4.75		15.75	4.75		15.75	V
Supply voltage, V_{BB}		5		60	5		60	V
Supply voltage, V_{SS}			0			0		V
High-level input voltage, V_{IH}	for V_{DD} = 5 V	3.5		5.3	3.5		5.3	V
	for V_{DD} = 15 V	13.5		15.3	13.5		15.3	
Low-level input voltage, V_{IL}		-0.3†		0.8	-0.3†		0.8	V
Continuous high-level output current, I_{OH}				-25			-25	mA
Operating free-air temperature, T_A		-40		85	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltages only.

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electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V to 15 V, V_{BB} = 60 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL4810BI			TL4810B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH} High-level output voltage	Q outputs	I_{OH} = -25 mA		57.5	58		57.5	58		V
	Serial output	V_{DD} = 5 V,	I_{OH} = -100 μA	4	4.5		4	4.5		
		V_{DD} = 15 V,	I_{OH} = -100 μA	14	14.7		14	14.7		
V_{OL} Low-level output voltage	Q outputs	I_{OH} = 1 μA,	Blanking input at V_{DD}		0.5	1		0.5	1	V
	Serial output	V_{DD} = 5 V,	I_{OL} = 100 μA		0.05	0.1		0.05	0.1	
		V_{DD} = 15 V,	I_{OL} = 100 μA		0.02	0.1		0.02	0.1	
I_{OL} Low-level Q output current (pull-down current)		V_O = 60 V, Blanking input at V_{DD}, T_A = MIN to 70°C		2.5	3.7		2.5	3.7		mA
		V_O = 60 V, Blanking input at V_{DD}, T_A = 85°C		2						
$I_{O(off)}$ Off-state output current		V_O = 0, Blanking input at V_{DD}, T_A = MAX			-1	-15		-1	-15	μA
I_H High-level input current		V_I = V_{DD}			30	50		30	50	μA
I_{BB} Supply current from V_{BB}		All outputs low			0.5	1		0.5	1	mA
		All outputs high, T_A = 0°C to MAX			2.7	4		2.7	4	
		All outputs high, T_A = -40°C				5				
I_{DD} Supply current from V_{DD}		All inputs at 0 V, V_{DD} = 5 V			10	50		10	50	μA
		One Q output high, V_{DD} = 15 V			10	100		10	100	
		All inputs at 0 V, V_{DD} = 5 V			10	50		10	50	
		All outputs low, V_{DD} = 15 V			10	100		10	100	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C, except for I_O.

timing requirements over recommended operating free-air temperature range

PARAMETER		V_{DD} = 5 V		V_{DD} = 15 V		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(CKH)}$	Pulse duration, clock high	250		50		ns
$t_{w(LEH)}$	Pulse duration, latch enable high	250		50		ns
$t_{su(D)}$	Setup time, data before clock↑	125		25		ns
$t_{h(D)}$	Hold time, data after clock↑	125		25		ns
$t_{CKH-LEH}$	Delay time, clock ↑ to latch enable high	125		25		ns

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, latch enable to output	V_{DD} = 5 V		1		μs
		V_{DD} = 15 V		0.5		

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PARAMETER MEASUREMENT INFORMATION
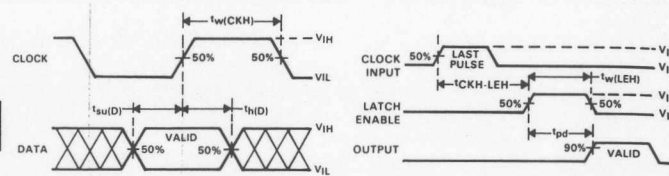
FIGURE 1. INPUT TIMING

FIGURE 2. OUTPUT SWITCHING TIMES

THERMAL INFORMATION
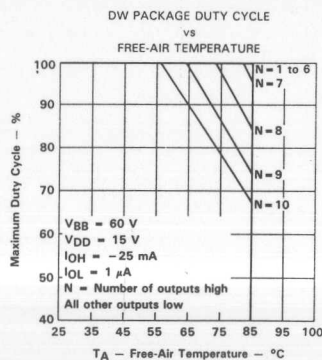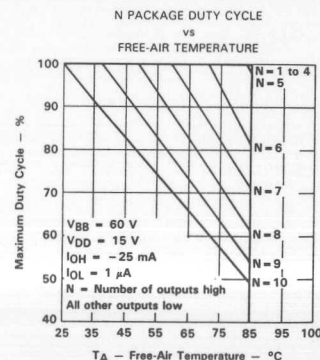
DW PACKAGE DUTY CYCLE
vs
FREE-AIR TEMPERATURE

$V_{BB} = 60$ V
$V_{DD} = 15$ V
$I_{OH} = -25$ mA
$I_{OL} = 1$ μA
N = Number of outputs high
All other outputs low

T_A — Free-Air Temperature — °C

FIGURE 3

N PACKAGE DUTY CYCLE
vs
FREE-AIR TEMPERATURE

$V_{BB} = 60$ V
$V_{DD} = 15$ V
$I_{OH} = -25$ mA
$I_{OL} = 1$ μA
N = Number of outputs high
All other outputs low

T_A — Free-Air Temperature — °C

FIGURE 4

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- Drives Up to 20 Lines
- 70-V Output Voltage Swing Capability
- 40-mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
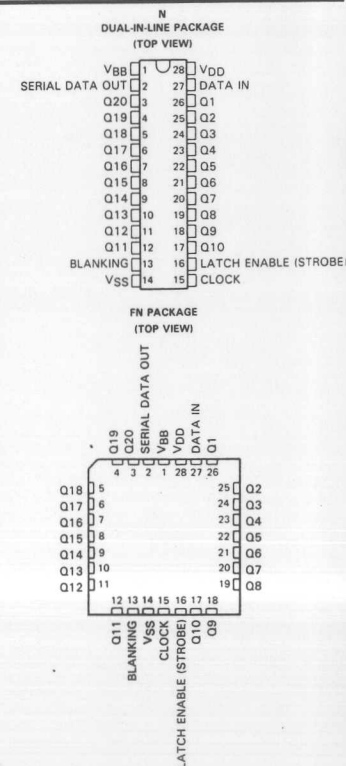- Direct Replacement for Sprague UCN5812A

description

The TL5812I and TL5812 are monolithic BIDFET[†] integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). Each device features a serial data output to cascade additional devices for large display arrays.

A 20-bit data word is serially loaded into the shift register on the low-to-high transition of the clock input. Parallel data is transferred to the output buffers through a 20-bit D-type latch while the Latch Enable input is high and is latched when the Latch Enable input is low. When the blanking input is high, all outputs are low.

The outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 volts and a source-current capability of 40 milliamperes. All inputs are CMOS compatible.

The TL5812I is characterized for operation from −40°C to 85°C. The TL5812 is characterized for operation from 0°C to 70°C.

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

V_{BB}	1	28	V_{DD}
SERIAL DATA OUT	2	27	DATA IN
Q20	3	26	Q1
Q19	4	25	Q2
Q18	5	24	Q3
Q17	6	23	Q4
Q16	7	22	Q5
Q15	8	21	Q6
Q14	9	20	Q7
Q13	10	19	Q8
Q12	11	18	Q9
Q11	12	17	Q10
BLANKING	13	16	LATCH ENABLE (STROBE)
V_{SS}	14	15	CLOCK

FN PACKAGE
(TOP VIEW)

Q19, Q20, SERIAL DATA OUT, V_{BB}, V_{DD}, DATA IN, Q1
4 3 2 1 28 27 26

Q18	5	25	Q2
Q17	6	24	Q3
Q16	7	23	Q4
Q15	8	22	Q5
Q14	9	21	Q6
Q13	10	20	Q7
Q12	11	19	Q8

12 13 14 15 16 17 18
Q11, BLANKING, V_{SS}, CLOCK, LATCH ENABLE (STROBE), Q10, Q9

[†] BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip — patented process.

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